SX-Aurora TSUBASA specifications

	Tower	Rack Mount			Supercomputer
Models					
Model name	A100-1	A300-2	A300-4	A300-8	A500-64
Max. Vector Engines (VEs)	1	2	4	8	64
# of Vector Hosts (VHs)	1	1	1	1	8
Form factor	Tower	1U rack mount	1U rack mount	4U rack mount	Proprietary rack
Vector Engine (VE)					
# of VEs	1	1, 2	1, 2, 4	6, 8	32, 48, 64
VE type	Type 10C	Type 10B/10C	Type 10B/10C	Type 10B/10C	Type 10A/10B
Max. VE performance (TFLOPS)	2.15	4.30	8.60	17.20	157.28
Max. VE memory bandwidth (TB/s)	0.75	2.40	4.80	9.60	76.80
Max. VE memory capacity (GB)	24	96	192	384	3072
Vector Host (VH)					
Xeon® processors/VH	1	1	2	2	2
Xeon® processor	Intel® Xeon® Gold 6100 Series, Silver 4100 Series				
Max. memory configuration	DDR4 DIMM x 6 / Xeon® processor				
Max. memory capacity (GB)	192	192	384	384	384
OS	Red Hat Enterprise Linux 7.3				
Interconnect					
Max. HCAs (InfiniBand EDR)	-	1	2	4	32
Bidirectional bandwidth (GB/s)	-	25	50	100	800
Power and Cooling					
Power consumption (HPL)	0.6 kW	0.9 kW	1.6 kW	2.8 kW	30 kW
Cooling	Air	Air	Air	Air	Water + Air
Software					
Bundled software	VE controlling software, VE driver				
Software Development Kit	Vector compiler/libraries/profiler/debugger for VE				
MPI	MPI library for VE				

Vector Engine(VE) Specifications

	Type 10A	Type 10B	Type 10C
Core Specifications			
Clock speed (GHz)	1.6	1.4	1.4
Peak performance (GFLOPS)	307.2	268.8	268.8
Average memory bandwidth (GB/s)	150	150	94
Processor Specifications			
# of cores / processor	8	8	8
Peak performance (TFLOPS)	2.45	2.15	2.15
Memory bandwidth (TB/s)	1.20	1.20	0.75
Cache capacity (MB)	16	16	16
Memory capacity (GB)	48	48	24

⚠ Safety Notice Before using this product, please read carefully and comply with the cautions and warnings in manuals such as the Installation Guide and Safety Precautions. Incorrect use may cause a fire, electrical shock, or injury.

Please visit SX-Aurora TSUBASA website for all the lastest updates:

SX-Aurora TSUBASA website
http://www.nec.com/en/global/solutions/hpc

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As of October 2017. Cat.No. E11-17100001E

\Orchestrating a brighter world NEC

Vector Supercomputer SX Series

SX-Aurora TSUBASA

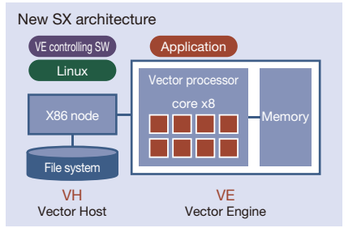
The new NEC supercomputer system "SX-Aurora TSUBASA" creates the future of HPC with a newly developed vector processor. Built as a PCIe card in a standard x86 environment, It combines "sustained performance" with ease of use.

Newly developed SX-Aurora TSUBASA architecture

•Vector processor + x86/Linux architecture

The new SX architecture contains the Vector Engine (VE) and Vector Host (VH). The VE executes complete applications while the VH mainly provides OS functions for connected VEs. The VE consists of one vector processor with eight vector cores, using "high bandwidth memory" modules (HBM2) for utmost memory bandwidth. The world's first implementation of one CPU LSI with six HBM2 memory modules using a "chip-on-wafer-on-substrate" technology (CoWoS) leads to the world-record memory bandwidth of 1.2 TB/s.

It is connected to the VH, a standard x86/Linux node, through PCIe. This new SX architecture, which executes an entire application on the VE and the OS on the VH, combines highest sustained performance, for which vector processors are famous, in a well-known x86/Linux environment.



Newly developed vector processor

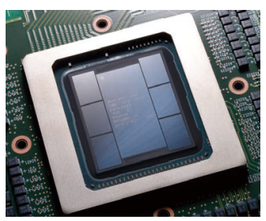
•Extremely high capability core and processor with extremely high memory bandwidth

The vector core on the VE processor is the most powerful single core in HPC as of today, thus keeping the design philosophy from the previous SX series. It will achieve industry leading calculation performance per core (307 GFLOPS)*1 and memory bandwidth per core (150 GB/s)*1.

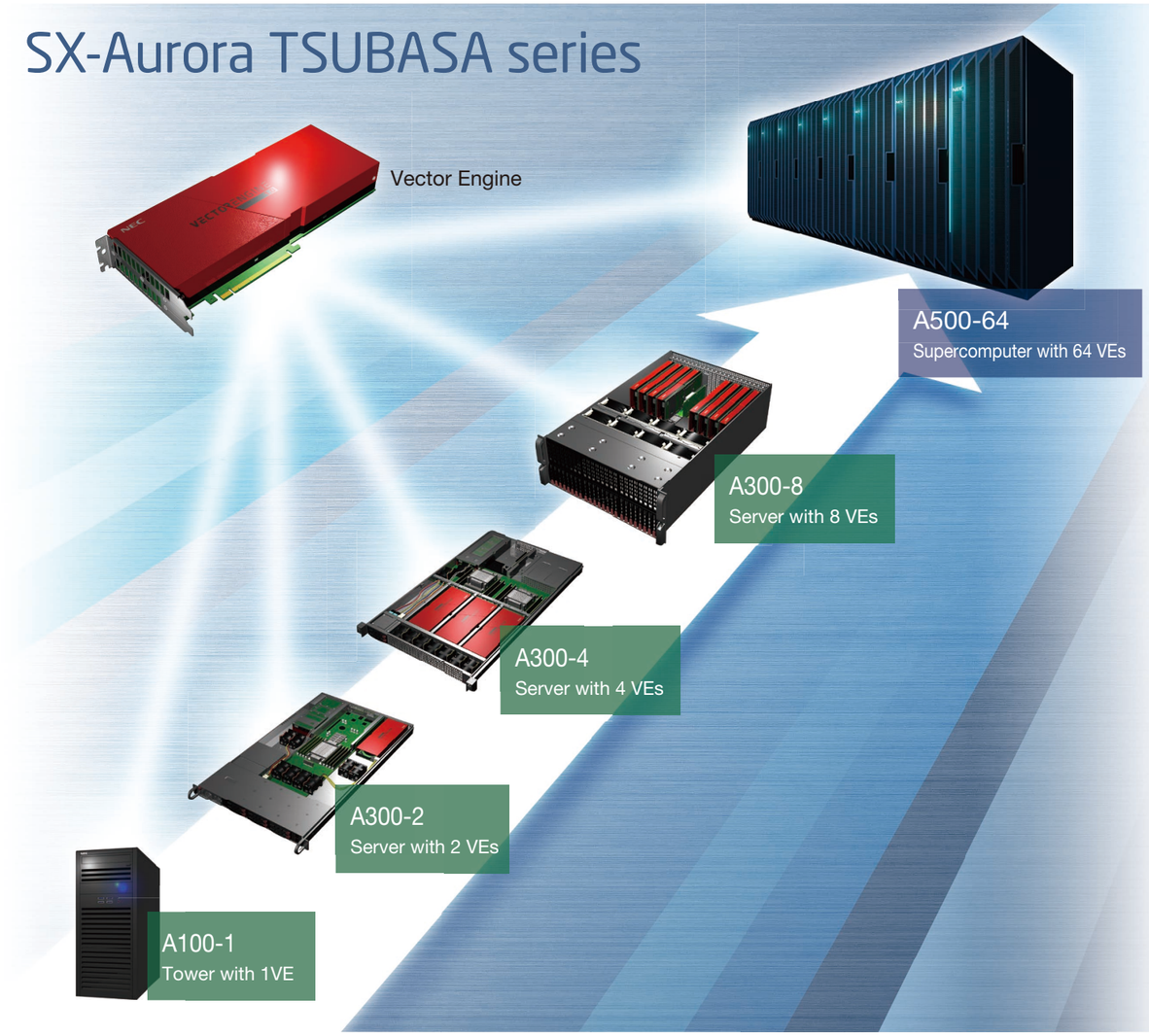
With eight cores the vector processor will execute applications with extremely high sustained performance. It features 2.45 TF peak performance and the world's highest memory bandwidth per processor, 1.2 TB/s. Different from standard processors a vector architecture is known to achieve a significant fraction of the peak performance on real applications.

•State of the art technology for high sustained performance

The vector processor employs 16nm FinFET process technology for extremely high performance and low power consumption.



SX-Aurora TSUBASA series



10x space efficiency and 5x power efficiency

The SX-Aurora TSUBASA offers up to 157 TF performance per rack and a memory bandwidth of up to 76 TB/s with 30 kW of power consumption, realizing 1/10 of the floor space and 1/5 of the power consumption compared to the predecessor SX-ACE.*2 This is a result of our innovation using cutting edge LSI and packaging technologies such as the CoWoS implementation, allowing for a thin wafer integration.

Inherited ease of use as a research and development tool

A supercomputer is a tool to increase the productivity of researchers and developers. For users to achieve the optimal vector-processor performance, the SX-Aurora TSUBASA offers the following major software features:

•Compiler with automatic vectorization and parallelization

Supporting a GNU environment, the SX-Aurora TSUBASA offers Fortran/C/C++ compilers with advanced automatic vectorization and parallelization for industry leading sustained performance and MPI libraries optimized for system configurations of the SX-Aurora TSUBASA.

•Rich scientific computing library

Scientific computing libraries optimized for SX-Aurora TSUBASA are available. These libraries include the industry standard BLAS, FFT, LAPACK, and ScaLAPACK.

From entry model to supercomputer model

VE cards with one vector-processor and high memory bandwidth HBM are used in a wide range of models. The product portfolio features a tower model that can be used on a user's desk to a supercomputer model for a large-scale supercomputer center. The product can be flexibly configured to meet the most demanding computational needs.

*1: as of October, 2017 (according to NEC's research), *2: Comparison in theoretical peak performance

Broad supercomputer -applicable targets